REMARKS

Claim 14 has been cancelled without prejudice or disclaimer and claims 1 and 6 have been amended.

Applicant respectfully requests further examination and reconsideration of claims 1-6 and 10-13 now pending in the application.

The Final Rejection mailed from the Patent office on January 26, 2004 has been carefully considered and indicates that:

a) Claims 6 and 10-14 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement;

b) Claims 1, 2, 4-6, and 14 are rejected under 35 § U.S.C. 102(b) as being anticipated by Akao;

c) Claims 1, 4, 6, and 14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Basset;

d) Claims 2, 3, 5, and 10-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Basset in view of Mattheis et al., Davidson et al., or applicant's admission at page 4, lines 4-10;

e) Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Akao; and

f) Claims 2, 5, and 10-13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Akao in view of Mattheis et al., Davidson et al., or

applicant's admission at page 4, lines 4-10.

In response to the Examiner's rejection of claims 6 and 10-14 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement:

1. With respect to claim 14, applicant has cancelled claim 14 without prejudice or disclaimer.

2. With respect to claim 6, applicant has amended claim 6 to delete "the programmable logic device comprising".

In view of the cancellation of claim 14 without prejudice or disclaimer, and the amendment made supra to claim 6 to delete "the programmable logic device comprising", applicant respectfully submits that the Examiner's grounds for the rejection of claims 6 and 10-14 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement no longer appear to be applicable and applicant therefore respectfully requests that the Examiner withdraw this rejection.

In response to the Examiner's rejection of claims 1, 2, 4-6, and 14 under 35 U.S.C. § 102(b) as being anticipated by Akao, and, the Examiner's rejection of claims 1, 4, 6, and 14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Basset, applicant has cancelled claim 14 without prejudice or disclaimer.

Regarding claim 1, applicant has amended claim 1 to describe that the configurable peripheral device includes a configurable logic block having circuitry capable of implementing a plurality of logic functions.

Regarding claim 6, applicant has amended claim 6 to describe that the plurality of peripheral devices are a plurality of configurable peripheral devices and that the configurable peripheral device includes a configurable logic block having circuitry capable of implementing a plurality of logic functions.

Explanation of support for the amendments made to claims 1 and 6 can be found at the end of the instant amendment.

Furthermore, pursuant to 37 CFR § 1.111(c), each of amended claims 1 and 6 describes the following advantageous distinctive feature that distinguishes over and avoids the prior art:

> "a configurable peripheral device comprising a configurable logic block having circuitry capable of implementing a plurality of logic functions"

Akao relies on a hardwired sequential processor to implement the different peripherals and Akao's does not teach or suggest that its peripheral devices have configurable logic blocks. Figures 15-17 of Akao describe a ROM and a RAM and Figure 20 is a hardwired control unit (see description of drawings cols. 9 -10). None of these figures disclose configurable logic blocks. Thus for at least this reason alone claims 1 and 6 should be allowable.

Basset discloses that a peripheral is programmed by setting an options register (col. 5, lines 27-38), not by configuring configurable logic blocks. Basset, does not teach or suggest that its peripheral devices have configurable logic blocks. Thus for at least this reason alone claims 1 and 6 should be allowable.

Regarding claims 2, 4, and 5, respectfully submits that since claims 2, 4, 5 depend from claim 1, claims 2, 4, and 5 should be allowable for at least the same reasons claim 1 is allowable.

In addition the Office Action's statement that claim 4 is anticipated by Basset as Figure 7 shows an FPGA is incorrect. Figure 7 shows a fixed logic device where signal 17 is a reset signal that connects option register memory elements 43 to a bus 15 and disconnects microprocessor 1 from the bus 15 (col. Col. 4, lines 37-54, and col. 7, lines 28-50).

In response to the Examiner's rejection of claims 2, 3, 5, and 10-13 under 35 U.S.C. § 103(a) as being unpatentable over

Basset in view of Mattheis et al., Davidson et al., or applicant's admission at page 4, lines 4-10, the Examiner's rejection of claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Akao, and, the Examiner's rejection of claims 2, 5, and 10-13 under 35 U.S.C. § 103(a) as being unpatentable over Akao in view of Mattheis et al., Davidson et al., or applicant's admission at page 4, lines 4-10, applicant respectfully submits that:

1. Regarding claims 2, 3, and 5, since claims 2, 3, and 5 ultimately depend from claim 1, claims 2, 3, and 5 should be allowable for at least the same reasons claim 1 is allowable.

2. Regarding claims 10-13, since claims 10-13 ultimately depend from claim 6, claims 10-13 should be allowable for at least the same reasons claim 6 is allowable.

In view of the arguments presented supra, applicant respectfully submits that the Examiner's grounds for the rejection of claims 2, 3, 5, and 10-13 under 35 U.S.C. § 103(a) as being unpatentable over Basset in view of Mattheis et al., Davidson et al., or applicant's admission at page 4, lines 4-10, the Examiner's grounds for the rejection of claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Akao, and, the Examiner's grounds for the rejection of claims 2, 5, and 10-13 under 35 U.S.C. § 103(a) as being unpatentable over Akao in view of Mattheis et al., Davidson et al., or applicant's admission at page 4, lines 4-10 no longer appear to be applicable and applicant therefore respectfully requests that the Examiner withdraw these rejections.

EXPLANATION OF SUPPORT

From paragraphs [0014] and [0015] and Figure 1 of the specification, and Chapter 3 of "The Programmable Logic Data Book 2000" published by Xilinx, Inc, the content of which has been incorporated by reference in the specification, and of which a copy was previously submitted in an IDS, one of ordinary skill in the art could make a configurable peripheral device

using at least one configurable logic block, where the configurable logic block has circuitry capable of implementing a plurality of logic functions such as, in one embodiment, a look-up-table (LUT) explained in Chapter 3 of "The Programmable Logic Data Book 2000". Thus there is support for the amendments made to claims 1 and 6.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on March 24, 2004

Pat Slaback
Name

Signature